WHAT IS CLAIMED IS:

1. A device formed in a semiconductor material of a first conductivity type, the semiconductor material having a dopant concentration, the device comprising:

a well of a second conductivity type formed in the semiconductor material, the well having a dopant concentration;

a first region of the second conductivity type formed in the well, the first region having a dopant concentration greater than the dopant concentration of the well, the first region being connected to a first node;

a second region of the first conductivity type formed in the well, the second region having a dopant concentration greater than the dopant concentration of the semiconductor material, the second region being connected to the first node;

a third region of the second conductivity type formed in the semiconductor material, the third region having a dopant concentration greater than the dopant concentration of the well, the third region being connected to a second node, and

a fourth region of the first conductivity type formed in the semiconductor material, the fourth region having a dopant concentration greater than the dopant concentration of the semiconductor material, the fourth region being connected to the second node, wherein the second region is reduced in size to reduce the number of minority carrier that are injected to at least a point where holding voltage is increased beyond the holding voltage of a conventional LVTSCR.

2. The device of Claim 1, wherein the first conductivity type is p type and the second conductivity type is n type.

3. The device of Claim 2, wherein the third region is increased in size to reduce space charge neutralization.

4. A method of manufacturing a device having an elevated holding voltage, and formed in a semiconductor material of a first conductivity type, the semiconductor material having a dopant concentration, comprising

a well of a second conductivity type formed in the semiconductor material, the well having a dopant concentration;

a first region of the second conductivity type formed in the well, the first region having a dopant concentration greater than the dopant concentration of the well, and being connected to a first node;

a second region of the first conductivity type formed in the well, the second region having a dopant concentration greater than the dopant concentration of the semiconductor material, and being connected to the first node;

a third region of the second conductivity type formed in the semiconductor material, the third region having a dopant concentration greater than the dopant concentration of the well, and being connected to a second node, and

a fourth region of the first conductivity type formed in the semiconductor material, the fourth region having a dopant concentration greater than the dopant concentration of the semiconductor material, and being connected to the second node, comprising

adjusting the size of the second region to limit injection of minority carriers to achieve the desired elevated holding voltage

5. The device of Claim 2, wherein the first conductivity type is p type and the second conductivity type is n type.

6. The method of Claim 5, wherein, in addition to adjusting the size of the second region, adjusting the size of the third region to increase electron injection to a point where space charge neutralization is sufficiently limited to achieve the desired elevated holding voltage.

7. A method of providing a device having a holding voltage substantially the same as a GGNMOS but supporting current densities that are at least twice as high as for a GGNMOS of substantially the same holding voltage, comprising providing an SCR-like structure having a p+ emitter that is sufficiently reduced in size so as to limit hole injection to the point where the space charge neutralization is so limited as to increase the holding voltage to the desired level.

8. A method of providing a device having a holding voltage substantially the same as a GGNMOS but supporting current densities that are at least twice as high as for a GGNMOS of substantially the same holding voltage, comprising providing a LVTSCR-like structure having a p+ emitter that is reduced in size below a predetermined value and having a n+ emitter that is increased in size to a point where the space charge neutralization is so limited as to increase the holding voltage to the desired level.

9. A method of providing a device having a higher holding voltage than a LVTSCR and supporting a higher current than a GGNMOS, comprising providing a LVTSCR-like structure having a p+ emitter that is sufficiently reduced in size so as to limit hole injection to the point where the space charge neutralization is so limited as to increase the holding voltage to the desired level.

10. A method of providing a device having a higher holding voltage than a LVTSCR and supporting a higher current than a GGNMOS, comprising providing a LVTSCR-like structure having a p+ emitter that is reduced in size below a predetermined value and having an n+ emitter that is increased in size to a point where the space charge neutralization is so limited as to increase the holding voltage to the desired level.